

Sub
A6

1. In a multiplexer which divides a carrier pulse train having a predetermined amplitude into N pulse trains, modulates said N pulse trains by N data signals, respectively, to produce modulated N pulse trains, and time-division multiplexes said modulated N pulse trains, the improvement comprising:
 - an amplitude adjuster which implements an amplitude adjustment so that said modulated N pulse trains have different amplitudes from each other.
2. The multiplexer according to claim 1, wherein said carrier pulse train has a period T between pulses thereof, and said modulated N pulse trains are time-division multiplexed with a phase difference of T/N.
3. The multiplexer according to claim 1, wherein said carrier pulse train is an optical carrier pulse train.
4. The multiplexer according to claim 1, wherein said N pulse trains are modulated by said N data signals through amplitude shift key modulation.
5. The multiplexer according to claim 1, wherein said N pulse trains are modulated by said N data signals through pulse code modulation.
6. In a demultiplexer which receives a multiplexed modulated pulse train produced by dividing a carrier pulse train having a predetermined amplitude into N pulse trains, modulating said N pulse trains by N data signals, respectively, to produce modulated N pulse trains, and time-division

multiplexing said modulated N pulse trains, and which extracts one of said modulated N pulse trains from said multiplexed modulated pulse train, the improvement comprising:

an amplitude detector for deriving an amplitude of one of said modulated N pulse trains which is extracted, said amplitude detector deriving said amplitude directly or indirectly from said extracted modulated pulse train; and

a judging circuit for identifying said extracted modulated pulse train based on said amplitude derived by said amplitude detector.

7. The demultiplexer according to claim 6, wherein said judging circuit comprises:

a mean amplitude detector for deriving a mean amplitude of said multiplexed modulated pulse train; and

a comparator for comparing the amplitude of said extracted modulated pulse train derived by said amplitude detector and the mean amplitude of said multiplexed modulated pulse train derived by said mean amplitude detector, so as to identify said extracted modulated pulse train.

8. The demultiplexer according to claim 6, wherein said carrier pulse train has a period T between pulses thereof, and said multiplexed modulated pulse train is obtained by time-division multiplexing said modulated N pulse trains with a phase difference of T/N , and

wherein said demultiplexer further comprises:

a passing/blocking circuit for passing said multiplexed modulated pulse train therethrough only when a voltage of a predetermined range is applied thereto, and for blocking said multiplexed modulated pulse train when a

voltage of other than said predetermined range is applied thereto;

a timing generator for generating a timing every T based on T/N of said multiplexed modulated pulse train;

a drive circuit which feeds a voltage of said predetermined range to said passing/blocking circuit per said timing generated by said timing generator so that one of said modulated N pulse trains passes through said passing/blocking circuit; and

a timing controller for controlling said timing generated by said timing generator so that the modulated pulse train identified by said judging circuit agrees with one of said modulated N pulse trains which is designated by an externally inputted select signal.

9. The demultiplexer according to claim 8, wherein said passing/blocking circuit converts said blocked multiplexed modulated pulse train into a current corresponding to an amplitude thereof, and said amplitude detector derives the amplitude of the extracted modulated pulse train based on said current fed from said passing/blocking circuit.

10. The demultiplexer according to claim 8, wherein N is 2, and wherein the voltage of said predetermined range of said passing/blocking circuit is periodically discrete relative to a voltage applied thereto, said timing generator produces a sine wave signal having the period T , said drive circuit adjusts the sine wave signal produced by said timing generator so that crest or trough portions of said sine wave signal reach the voltage of said predetermined range of said passing/blocking circuit to cause one of the two modulated pulse trains passes through said passing/blocking circuit, and said timing controller adds a given DC bias voltage to the sine wave signal produced by said timing

~~through
edetermin
ultiplexe
l carrier~~

- A

12. A multiplex communication system comprising:

a demultiplexer which receives said multiplexed modulated pulse train

an amplitude detector for deriving an amplitude of one of said

a judging circuit for identifying said extracted modulated pulse train

add A6 } based on said
add C1 }